#24/Appeal Brief 12/8/03

PATENT
Docket No.: M4065.0321/P321-A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of: Pai-Hung Pan, et al.	
Serial No.: 09/577,835	Examiner: C. Nguyen
Filed: May 25, 2000	Group Art Unit: 2811
For: PASSIVATION OF SIDEWALLS OF A WORD LINE STACK	

Assistant Commissioner for Patents
Washington, D.C. 20231

APPELLANTS' BRIEF ON APPEAL

Sir:

This is an appeal pursuant to 35 U.S.C. § 134 and 37 C.F.R. §§ 1.191 et seq. from the final rejection of claims 25 – 30 of the above-identified application mailed July 9, 2003. The fee for submitting this Brief ($330.00, 37 C.F.R. § 1.17(c)) is attached hereto. Any deficiency in the fees associated with this Brief should be charged to our Deposit Account No. 04-1073. The Notice of Appeal was filed on September 17, 2003. Enclosed with this original are two copies of this brief.

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I. Real Party in Interest

The real party in interest in this appeal is Micron Technology, Inc., a Corporation of Delaware, the assignee of this application.

II. Related Appeals and Interferences

There are no related appeals or interferences.

III. Status of Claims

Claims 25 – 27 and 30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Gardner (U.S. Patent No. 5,899,721) in view of Mogami (U.S. Patent No. 5,656,519). Claims 28 – 29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Gardner in view of Mogami and Bai (U.S. Patent No. 5,861,340).

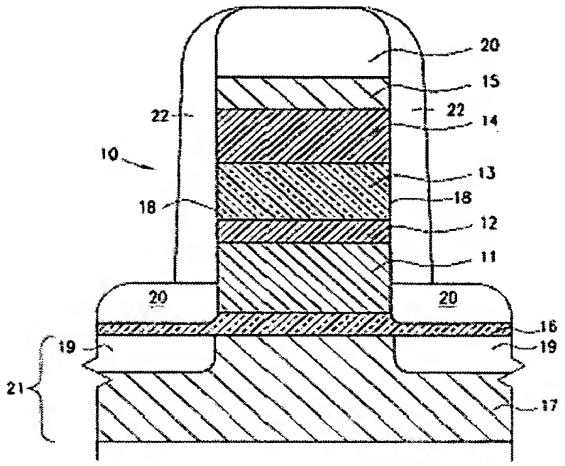
IV. Status of Amendments

No amendments have been filed subsequent to the final rejection on June 20, 2003. Therefore, the claims set forth in the appendix to this brief are those which have been finally rejected.

V. Summary of Invention

The present invention is directed to an integrated circuit. Referring to, for example, Fig. 4 (right), it can be seen that the integrated circuit includes a gate electrode stack 10 disposed upon a dielectric film 16. The gate electrode stack 10 is formed over a portion of a wafer, such as substrate 17. The gate stack 10 includes a plurality of layers, for example, layers 11, 12, 13, 14, and 15. Above the gate stack 10 is an oxide cap 20. In one embodiment, the electrode stack 10 includes a polysilicon layer 11 and at least one metal layer 13. As shown in the figures, the sidewalls 18 of the electrode stack are continuously vertical. Surrounding the sidewalls 18, continuously from the bottom to the top of the sidewalls 18 are composite spacers, each of which comprise a nitride spacer 22 stacked above an oxide spacer 20. The oxide spacer 20 extends from at least a bottom most portion of the continuously vertical sidewalls 18 to an intermediate point between the bottom most portion of the sidewalls 18 and a top point of the sidewalls 18. The nitride spacer 22, which is formed after the oxide spacer 20 is formed, extends from the intermediate point to the top of the sidewalls 18.

FIG. 4



VI. Issue

A. Whether claims 25 – 27 and 30 are properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Gardner in view of Mogami.

B. Whether claims 28 – 29 are properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Gardner in view of Mogami and further in view Bai.

VII. Grouping of Claims

Claims 25 – 30 stand and fall together.

VIII. Argument

As Appellants discuss in detail below, the Final Rejection of claims 25 – 30 is devoid of any factual or legal premise that supports a position of unpatentability. It is respectfully submitted that the Final Rejection does not even meet the threshold burden of presenting a prima facie case of unpatentability. For this reason alone, Appellant is entitled to reversal of the rejection. In re Oetiker, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992).

A. THE SUBJECT MATTER DEFINED IN CLAIMS 25 – 27 AND 30 WOULD NOT HAVE BEEN OBVIOUS OVER GARDNER IN VIEW OF MOGAMI BECAUSE THERE IS NO MOTIVATION TO COMBINE THE REFERENCES AS SUGGESTED IN THE OFFICE ACTION, AND FURTHER, EVEN IF THE REFERENCES WERE COMBINED AS SUGGESTD, THE RESULTING STRUCTURE WOULD NOT CORRESPOND TO THE CLAIMED INVENTION

Independent claim 25 recites "wherein each of said composite spacers further comprises a nitride spacer vertically stacked above an oxide spacer, said oxide spacer extending along the bottom of said continuously vertical sidewalls to an intermediate point in between the top and the bottom of said continuously vertical sidewalls, and said nitride space spacer extending from the intermediate point to the top of said continuously vertical sidewalls."

Gardner at Figs. 8 – 9 (right) teaches a method of fabricating a semiconductor device having small spacers and including a gate stack comprised of a gate oxide (i.e., in Fig. 9, the layer located immediately under 104), a polysilicon gate conductor 104, and a metal silicide 122. Gardner discloses the formation of a composite spacer along a continuously vertical sidewall with the composite spacer having a nitride layer 114 over an oxide layer 116. As shown in Fig. 9, the composite spacer fails to "extend[] continuously from a bottom to a top of said continuously vertical sidewalls," as required by claim 25. Specifically, the composite spacer fails to extend to the top of the vertical sidewall of metal silicide layer 122.

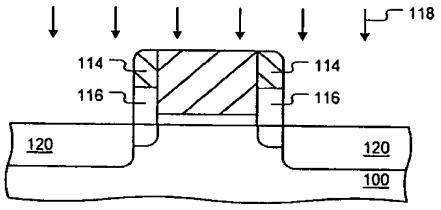


FIG. 8

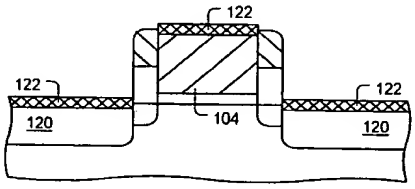
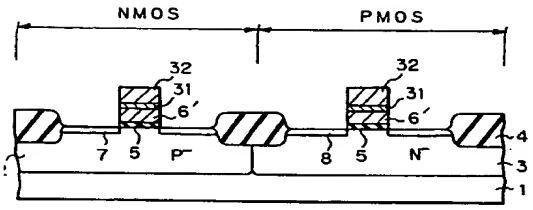


FIG. 9

Fig. 8A



Mogami is directed to a method of manufacturing a MOS device having a gate electrode and source/drain regions. Mogami at Fig. 8a (right) discloses the formation of a gate electrode stack by depositing: a gate oxide layer 5, a polysilicon layer 6', a tungsten nitride layer 31, and a second polysilicon layer 32. In Fig. 8B of Mogami (not shown), a simple (i.e., single material, or non-composite) oxide spacer 9 is formed which spans the sidewalls of the electrode stack under construction (i.e., layers 5, 6', 31, and 32). In Mogami Fig. 8C (not shown), the polysilicon layer 32 of the electrode stack under construction (only) is removed, thereby causing the top portion of the oxide spacer 9 to exceed the height of the top portion of the electrode stack under construction (which now has a top at layer 31).

Fig. 8D

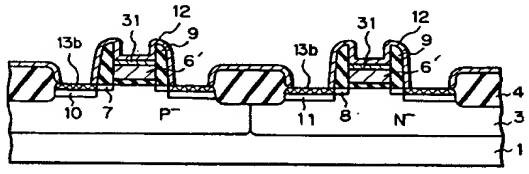


Fig. 8E

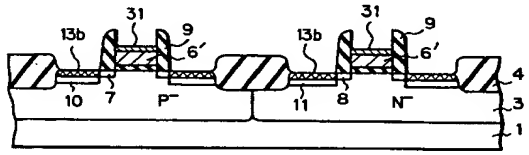
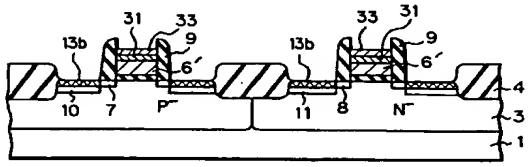


Fig. 8F



In Mogami Figs. 8D, 8E, and 8F (right), a titanium layer is deposited and reacted, the unreacted portions of the titanium layer are removed, and finally a tungsten layer is deposited, respectively. The completed device is illustrated in Fig. 8F, and still retains an oxide sidewall 9 higher than the top of the electrode stack (now tungsten layer 33). Mogami further discloses that having an oxide spacer which extends above the height of the gate electrode stack electrically isolates the gate electrode stack from the source/drain regions and therefore is

advantageous in preventing short circuits between the gate electrode stack and the source/drain regions. Mogami at column 8, lines 5-15.

Mogami fails to disclose or suggest "a plurality of composite spacers each extending continuously from a bottom to a top of said continuously vertical sidewalls, wherein each of said composite spacers further comprises a nitride spacer vertically stacked above an oxide spacer," as required by claim 25. Mogami further fails to disclose or suggest "said oxide spacer extending along the bottom of said continuously vertical sidewalls to an intermediate point in between the top and the bottom of said continuously vertical sidewalls," which is also required by claim 25.

i. THERE IS NO MOTIVATION TO COMBINE THE MOGAMI AND GARDNER REFERENCES.

The Final Rejection alleges that it would have been obvious to "form the spacer structure extending from a bottom to over a top of the continuously vertical sidewalls of [the] gate electrode stack as taught by Mogami into Gardner et al.'s device in order to prevent the short circuit between the source/drain regions and gate electrode stack." Final Rejection at page 3. However, such a conclusion is defective for at least the following two reasons.

First, Gardner already includes a mechanism for avoiding short circuits between source/drain regions and the gate electrode stack. Referring again to Gardner Fig. 9 (above), it can be seen that the source/drain regions 120 and the top of the gate electrode stack are enclosed by metal silicide layers 122. The metal silicide layers 122 are formed in a process described at column 7, lines 12-41. More specifically, Gardner states at column 7, lines 33-41:

> The resulting metal silicide 122 has a relatively low resistivity and serves as a self-aligned contact region across source/drain regions 120 and gate conductor 104. Absent

> refractory metal upon the lower portions of the spacers, no silicide formation occurs at those potions. Consequently, silicide bridging between gate conductor 104 and source/drain regions 120 is less likely to occur.

As Gardner already incorporates a mechanism to prevent short circuits between the gate electrode stack and source/drain regions, there would be no need to incorporate the spacer structure of Mogami into the gate electrode stack of Gardner for performing the same function.

Second, the spacer structure of Gardner is a composite oxide-nitride spacer while the spacer of Mogami is a simple oxide spacer. If the oxide portion of the composite spacer were lengthened as suggested to achieve the benefit taught by Mogami there would be no need for the nitride portion of the spacer in the Gardner structure.

ii. COMBINING THE MOGAMI AND GARDNER REFERENCES WOULD NOT HAVE RESULTED IN THE CLAIMED INVENTION

Further, even if the teachings of Mogami and Gardner could be combined as suggested in the Final Rejection, the resulting gate electrode stack would not correspond to the claimed invention. The gate electrode stack achieved by combining the teachings of the Mogami and Gardner references would include a sidewall having an oxide layer that runs from at least a bottom of the stack to above a top of the sidewall. Such a structure would not be the claimed structure because claim 25 requires "composite spacers" further comprising "a nitride spacer vertically stacked above an oxide spacer," with the oxide spacer "extending along the bottom of said continuously vertical sidewalls to an intermediate point in between the top and the bottom of said continuously vertical sidewalls" and "said nitride space spacer extending from the intermediate point to the top of said continuously vertical sidewalls." (emphasis added).

Thus, the combination of Mogami and Gardner does not render claim 25 obvious. Claims 26-27 and 30 depend from claim 25 and are allowable along with claim 25.

B. THE SUBJECT MATTER DEFINED IN CLAIMS 28 – 29 WOULD NOT HAVE BEEN OBVIOUS OVER GARDNER IN VIEW OF MOGAMI AND BAI BECAUSE THERE IS NO MOTIVATION TO COMBINE THE REFERENCES AS SUGGESTED IN THE OFFICE ACTION, AND FURTHER, EVEN IF THE REFERENCES WERE COMBINED AS SUGGESTD, THE RESULTING STRUCTURE WOULD NOT CORRESPOND TO THE CLAIMED INVENTION

Claims 28 – 29 depend from claim 25 and are allowable for at least the same reasons as set forth above with respect to claim 25.

IX. Conclusion

In Conclusion, Appellant respectfully submits that the Final Rejection of claims 25 - 30 is in error for at least the reasons given above and should, therefore, be reversed.

Dated: November 17, 2003

Respectfully submitted,

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APPENDIX

25. An integrated circuit comprising:

a semiconductor substrate;

a gate dielectric film disposed on a surface of the substrate;

a gate electrode stack disposed on the gate dielectric film, wherein the stack includes a plurality of layers located over the gate dielectric film and forms continuously vertical sidewalls; and

a plurality of composite spacers each extending continuously from a bottom to a top of said continuously vertical sidewalls,

wherein

each of said composite spacers further comprises a nitride spacer vertically stacked above an oxide spacer,

said oxide spacer extending along the bottom of said continuously vertical sidewalls to an intermediate point in between the top and the bottom of said continuously vertical sidewalls, and

said nitride space spacer extending from the intermediate point to the top of said continuously vertical sidewalls.

26. The integrated circuit of claim 25 wherein the stack includes a polysilicon layer on the gate dielectric film and a metal layer above the polysilicon layer, and wherein the spacers extend along sidewalls of the metal layer.

27. The integrated circuit of claim 26 wherein the metal layer comprises a material selected from a group consisting of a refractory metal or a refractory metal alloy.

28. The integrated circuit of claim 26 wherein the stack includes a conductive barrier layer between the polysilicon layer and the metal layer, and where the spacers extend along sidewalls of the barrier layer.

29. The integrated circuit of claim 28 wherein the barrier layer is substantially impermeable to silicon and metal atoms.

30. The integrated circuit of claim 25 wherein the spacers have a thickness in the range of about 50 Å to about 500 Å.